IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Akhil K. Garlapati et al.		
Title:	VOLTAGE REFERENCE GENERATOR CIRCUIT USING LOW-BETA EFFECT OF A CMOS BIPOLAR TRANSISTOR		
Application No.:	10/813,837	Filed:	March 31, 2004
Examiner:	Rajnikant B. Patel	Group Art Unit:	2838
Atty. Docket No.:	026-0044	Confirmation No.:	6047

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APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal, filed on January 9, 2007. The fee required under 37 C.F.R. § 41.20(b)(2) is being paid as directed in an electronic submission of this paper.

REAL PARTY IN INTEREST

The real party in interest in this appeal is Silicon Laboratories Inc., the assignee of record, as evidenced by the assignment recorded at Reel/Frame 015173/0365.

RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any prior and pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision of this appeal.

STATUS OF CLAIMS

Claims 1, 7-26, 28-37, 55-60 are pending. Claims 1, 7-26, 28-37, 55-60 stand as rejected, claims 38-54 have been withdrawn. Rejected claims 1, 7-26, 28-37, 55-60 are the subject of this appeal.

STATUS OF AMENDMENTS

A Response After Final Rejection, presenting arguments without amendments, was filed on November 29, 2006. A Supplemental Amendment was filed on March 2, 2007 to cancel claims 4-6 and to correct antecedent basis of claim 29. The above-mentioned status of claims and the Claims Appendix reflect these amendments.

SUMMARY OF CLAIMED SUBJECT MATTER

The independent claims involved in this appeal are claims 1, 26, 55, and 59. Subject matter defined in those claims is directed to voltage reference generator circuits. Referring to Fig. 2, voltage reference generator 200 includes bipolar transistor 206 that is coupled in a diode configuration and coupled to ground. See paragraph 1019. Bipolar transistor 208 is configured as an amplifier. See paragraph 1019. Referring to Fig. 3, in another embodiment of the present invention, instead of coupling the base of transistor 206 to ground, transistor 206 may be coupled to node 330 and biased by transistors 332 and 334. See paragraph 1019. Similarly, base resistor R_3 may be coupled to node 330 to receive the bias voltage generated by transistors 332 and 334. See paragraph 1019.

Referring back to Fig. 2, the saturation currents of transistor 208 and transistor 206 vary by a factor of M. See paragraph 1020. Operational amplifier 214 maintains equivalent voltages at nodes 218 and 220, i.e., $V_{218} = V_{220} = V_{BE206}$. See paragraph 1020. Hence, the difference between V_{BE206} and V_{BE208} , i.e., $\Delta V_{BE206,208}$, forms across resistor R_3. See paragraph 1020.

$$I_{B208} = \frac{V_{BE206} - V_{BE208}}{R_3}$$ and

$$I_2 = I_{E208} = (\beta_{208}+1)I_{B208} = (\beta_{208}+1)\frac{V_{BE206}-V_{BE208}}{R_3} = (\beta_{208}+1)\frac{V_T \ln\left(\frac{M}{N}\right)}{R_3},$$

where N = W_{204}/W_{202}, W_{204} being the width of transistor 204 and W_{202} being the width of transistor 202 and the channel lengths of transistor 204 and transistor 202 being substantially equal. See paragraph 1020. Since the thermal voltage V_T has a positive temperature coefficient k/q, the current proportional to the voltage difference is proportional to an absolute temperature, i.e., I_2 is a ptat current. See paragraph 1020.

Transistor 212 provides a ctat voltage, V_{BE212}. See paragraph 1021. By compensating the ptat current with a ctat voltage, transistors 202, 204, 206, 208, and 212, and resistors R_1 and R_2, may be appropriately sized to generate a substantially constant reference voltage output, i.e., V_{REF}:

$$\frac{V_{REF}-V_{BE212}}{R_4} = I_2$$

$$V_{REF} = V_{BE212} + I_2 R_4$$

$$V_{REF} = V_{BE212} + (\beta_{208}+1)\frac{R_4 V_T \ln\left(\frac{M}{N}\right)}{R_3}.$$

See paragraph 1021. In other embodiments, a ctat current may be formed and summed with I_2 to create a substantially constant current. See paragraph 1021. Note that the beta of a bipolar transistor has a dependence on temperature. See paragraph 1021. Thus V_{REF} may be modeled as a quadratic function of temperature:

$$V_{REF} = aT^2 + bT + c,$$

where a, b, and c are greater than zero. See paragraph 1021. In general, a, b, and c are determined according to target process technology, supply voltage, and reference voltage. See paragraph 1021. Note that in a typical CMOS process, parasitic substrate pnp transistors (e.g., in the case of an n-well process) and parasitic substrate npn transistors (e.g., in the case of a p-well

process) may be used as bipolar transistors. See paragraph 1021. These transistors have a low-beta (e.g., $\beta < 10$) as compared to transistors formed in a bipolar process (e.g., $\beta > 100$). See paragraph 1021. Thus currents produced by amplifying a base current of the CMOS bipolar transistor are manageable by typical CMOS devices. See paragraph 1021.

Voltage reference generator 200 benefits from the low-beta of parasitic bipolar transistors by reducing noise on V_{REF}. See paragraph 1022. In voltage reference 200, the ptat current, i.e., current I_2, is generated by amplifying the base current of transistor 208, which is a ptat current. See paragraph 1022. Current I_2 itself is not amplified. See paragraph 1022.

In some exemplary applications, it may be advantageous to generate a V_{REF} that varies with temperature. See paragraph 1024. The ratio of R_4/R_3 may be adjusted to provide a slope appropriate to the typical application by strategically positioning the center of the parabola. See paragraph 1024. For example, by appropriately positioning a vertex of the parabola, the slope of V_{REF} as a function of temperature may be adjusted to generate a V_{REF} that always increases or always decreases as a function of temperature under particular operating conditions. See paragraph 1024.

Claim 55 is directed to an apparatus including a means for developing a current proportional to absolute temperature. The means for developing the current proportional to absolute temperature includes a resistor coupled to a base of a first bipolar transistor, a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities being formed across the resistor. A corresponding structure includes resistor R_3, transistor 208, transistor 206, operational amplifier 214, transistor 202, and transistor 204 of Figs. 2 and 3. The apparatus includes a means for amplifying the current. The means for amplifying includes the first bipolar transistor. A corresponding structure includes transistor 208. The apparatus also includes a means for generating a reference voltage based at least in part on the amplified current. A corresponding structure includes transistor 210, resistor R_4, and transistor 212 of Figs. 2 and 3.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Ground I: The rejection of claim 26 under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 5,949,255 to Sawtell.

Ground II: The rejection of claims 7-26, 28-37, and 55-60 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,949,255 to Sawtell in combination with U.S. Patent No. 5,568,045 to Koazechi.

Ground III: The rejection of claims 1, 3, 7-26, 28-37, 55-57, and 59-60 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,563,502 to Akioka et al. in combination with U.S. Patent No. 5,568,045 to Koazechi.

ARGUMENT

Ground I: Claim 26 stands rejected under 35 U.S.C. § 102 as being unpatentable over U.S. Patent No. 5,949,255 to Sawtell. In rejecting claim 26, the Examiner engages in an improper analysis under 35 U.S.C. § 102(b) because Sawtell fails to teach each element of the claimed combination.

Under 35 U.S.C. § 102, each element of a claim must be found in the single prior art reference, either expressly or inherently. See Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1565, 24 USPQ2d (BNA) 1321, 1326 (Fed. Cir. 1992). A reference teaches an element inherently if the "prior art necessarily functions in accordance with, or includes, the claimed limitations." See MEHL/Biophile Int'l Corp. v. Milgraum, 192 F.3d 1362, 1364, 52 USPQ2d (BNA) 1303, 1305 (Fed. Cir. 1999). If the reference fails to teach even one limitation of a claim, then the claim is not anticipated. See Kloster Speedsteel AB v. Crucible Inc., 848 F.2d 1560, 7 USPQ2d (BNA) 1507 (Fed. Cir. 1986).

Claim 26

Applicants respectfully maintain that Sawtell, alone or in combination with other references of record, fails to teach or suggest

> a base current proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of a first bipolar transistor, the voltage difference being formed across a first resistor coupled to a base of the first bipolar transistor,

as required by claim 26. Sawtell is directed to an adaptive gain optocoupler circuit that includes a feedback control circuit. See col. 6, lines 51-60. The Office relies on Figs. 1-4, col. 1, lines 60-69, and col. 9, lines 34-45 of Sawtell to teach the limitations of claim 26. Sawtell teaches an exponential transconductance stage that converts a voltage control signal, V_C, into an output current signal, I_C, which is exponentially related to a differential voltage. See col. 7, lines 7-44; col. 8, lines 29-34; Figs. 3 and 4. The exponential transconductance stage of Sawtell includes differential input voltage generation circuit 465 that applies a voltage ΔV across base terminals of transistors 425 and 426. See col. 9, lines 14-35. The voltage ΔV of Sawtell is not formed across a resistor as required by claim 26. The voltage across resistor 407 of Sawtell is 5 Volts. See col. 9, lines 9-11. The voltage across resistor 413 of Sawtell is 5 Volts - $4V_{DR}$, where V_{DR} is the voltage drop across a pn junction diode. See col. 8, lines 53-55; col. 9, lines 38-46. Resistor 412 of Sawtell is coupled to the emitter of transistor 437 to form a portion of a current source. See col. 9, lines 35-38. The voltages across resistors 407, 412, and 413 fail to teach or suggest a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of a first bipolar transistor, as required by claim 26. Nowhere does Sawtell teach or suggest a base current proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of a first bipolar transistor, the voltage difference being formed across a first resistor coupled to the base of the first transistor, as required by claim 26. Since Sawtell does not disclose or suggest that limitation and no other art of record adds the missing disclosure, Applicants respectfully maintain that the rejection of claim 26 and all claims dependent thereon, be reversed.

Ground II:

Claims 3, 7-26, 28-37, and 55-60 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,949,255 to Sawtell in combination with U.S. Patent No. 5,568,045 to Koazechi.

In rejecting the claims, the Examiner engages in an examination that fails to establish a *prima facie* case of obviousness because the references fail to teach or suggest the claimed combination. See In re Nielson, 816 F.2d 1567, 1572, 2 USPQ2d (BNA) 1525, 1528 (Fed. Cir. 1987); see also In re Kahn, 441 F.3d 977, 986, 78 USPQ2d (BNA) 1329, 1335 (Fed. Cir. 2006).

In general, obviousness is a legal determination based on underlying factual inquiries. See Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1572-73, 24 USPQ2d (BNA) 1321, 1332-33 (Fed. Cir. 1992). Graham v. John Deere Co., 383 U.S. 1, 17 (1966) defines the factual inquiries utilized to evaluate the prior art. Specifically, the prior art is evaluated in terms of: (1) its scope and content; (2) the differences between the prior art and the claimed invention; (3) the level of ordinary skill in the art at the time the application was filed; and (4) objective, or secondary, evidence of nonobviousness such as commercial success, failure of others, long-felt need and unexpected results, which must be considered in reaching a conclusion of obviousness. See Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ (BNA) 459, 460 (1966); Panduit Corp. v. Dennison Mfg. Co., 810 F.2d 1561, 1566-67, 1 USPQ2d (BNA) 1593, 1595-96 (Fed. Cir. 1987); Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1573, 24 USPQ2d (BNA) 1321, 1333 (Fed. Cir. 1992).

In the present appeal, the issue relates to specific differences between the prior art and appealed claims. All claim limitations must be considered in the obviousness analysis. See Panduit Corp., 810 F.2d at 1576, 1 USPQ2d at 1603–04. None of the references, standing alone or in combination, teach all of the recited limitations.

Claims 26, 28-37, and 60

Regarding claim 26, Applicants respectfully maintain that Sawtell, alone or in combination with Koazechi, fails to teach or suggest

> a base current of a first bipolar transistor, the base current being proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of the first bipolar transistor, the voltage difference being formed across a first resistor coupled to a base of the first bipolar transistor,

as required by claim 26. Sawtell fails to teach or suggest the claimed limitation, as argued above with regards to Ground I. Koazechi fails to compensate for the shortcomings of Sawtell. Koazechi teaches the voltage difference DVBE between base-emitter voltages VBE20 and VBE24 of transistors 20 and 24, which appears across resistor 2. See col. 4, lines 14-21. Resistor 2 of Koazechi is coupled to the emitter of transistor 24. See Fig. 2. Nowhere does Koazechi teach or suggest a base current of a first bipolar transistor, the base current being proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of the first bipolar transistor, the voltage difference being formed across a first resistor coupled to a base of the first bipolar transistor, as required by claim 26. Since neither Sawtell nor Koazechi alone or in combination teaches or suggests the limitations of claim 26, Applicants respectfully request that the rejection of claim 26 and all claims dependent thereon, be reversed.

Claim 59

Regarding claim 59, the Office action fails to point out where Sawtell and/or Koazechi teach or suggest, and Applicants respectfully maintain that Sawtell, alone or in combination with Koazechi and/or other references of record, fails to teach or suggest

> a base-collector voltage of a first bipolar transistor equal to a voltage difference between two base-emitter voltages biased at different current densities,

as required by claim 59. Since neither Sawtell nor Koazechi teaches or suggests the limitations of claim 59, Applicants respectfully request that the rejection of claim 59 and all claims dependent thereon, be reversed.

Claims 3 and 7-25

Regarding claims 3 and 7-25, Applicants respectfully maintain that Sawtell, alone or in combination with Koazechi, fails to teach or suggest

> a base current proportional to a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities, the voltage difference being formed across a resistor coupled to the base of the first bipolar transistor,

as required by claim 1, from which claims 3 and 7-25 depend. Sawtell is directed to an adaptive gain optocoupler circuit that includes a feedback control circuit. See col. 6, lines 51-60. The Office apparently relies on Figs. 1-4, col. 1, lines 60-69, and col. 9, lines 34-45 of Sawtell to teach the limitations of claim 1. Sawtell teaches an exponential transconductance stage that converts a voltage control signal, V_C, into an output current signal, I_C, which is exponentially related to a differential voltage. See col. 7, lines 7-44; col. 8, lines 29-34; Figs. 3 and 4. The exponential transconductance stage of Sawtell includes differential input voltage generation circuit 465 that applies a voltage ΔV across base terminals of transistors 425 and 426. See col. 9, lines 14-35. The voltage ΔV of Sawtell is not formed across a resistor as required by claim 1. The voltage across resistor 407 of Sawtell is 5 Volts. See col. 9, lines 9-11. The voltage across resistor 413 of Sawtell is 5 Volts - $4V_{DR}$, where V_{DR} is the voltage drop across a pn junction diode. See col. 8, lines 53-55; col. 9, lines 38-46. Resistor 412 of Sawtell is coupled to the emitter of transistor 437 to form a portion of a current source. See col. 9, lines 35-38. The voltages across resistors 407, 412, and 413 fail to teach or suggest a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities, as required by claim 1. Nowhere does Sawtell teach or suggest a base current proportional to a voltage difference between two base-emitter voltages of bipolar transistors configured to have

different current densities, the voltage difference being formed across the resistor coupled to the base of the first bipolar transistor, as required by claim 1.

Koazechi fails to compensate for the shortcomings of Sawtell. Koazechi teaches the voltage difference DVBE between base-emitter voltages VBE20 and VBE24, which appears across resistor 2. Col. 4, lines 14-21. Resistor 2 of Koazechi is coupled to the emitter of transistor 24. Figure 2. Nowhere does Koazechi teach or suggest a base current proportional to a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities, the voltage difference being formed across the resistor coupled to the base of the first bipolar transistor, as required by claim 1. Since neither Sawtell nor Koazechi teaches or suggests the limitations of claim 1, Applicants respectfully request that the rejection of claims 3 and 7-25, be reversed.

Claims 55-58

Regarding claim 55, Applicants respectfully maintain that Sawtell, alone or in combination with Koazechi, fails to teach or suggest that

> a means for developing the current proportional to absolute temperature includes a resistor coupled to a base of the first bipolar transistor, a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities being formed across the resistor,

as required by claim 55. Sawtell is directed to an adaptive gain optocoupler circuit that includes a feedback control circuit. See col. 6, lines 51-60. The Office apparently relies on Figs. 1-4, col. 1, lines 60-69, and col. 9, lines 34-45 of Sawtell to teach the limitations of claim 55. Sawtell teaches an exponential transconductance stage that converts a voltage control signal, V_C, into an output current signal, I_C, which is exponentially related to a differential voltage. See col. 7, lines 7-44; col. 8, lines 29-34; Figs. 3 and 4. The exponential transconductance stage of Sawtell includes differential input voltage generation circuit 465 that applies a voltage ΔV across base terminals of transistors 425 and 426. See col. 9, lines 14-35. The voltage ΔV across resistor 407

of Sawtell is not formed across a resistor as required by claim 55. The voltage across resistor 407 of Sawtell is 5 Volts. See col. 9, lines 9-11. The voltage across resistor 413 of Sawtell is 5 Volts - $4V_{DR}$, where V_{DR} is the voltage drop across a pn junction diode. See col. 8, lines 53-55; col. 9, lines 38-46. Resistor 412 of Sawtell is coupled to the emitter of transistor 437 to form a portion of a current source. See col. 9, lines 35-38. The voltages across resistors 407, 412, and 413 fail to teach or suggest a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities as required by claim 55. Nowhere does Sawtell teach or suggest a means for developing a current proportional to absolute temperature that includes a resistor coupled to a base of a first bipolar transistor, a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities being formed across the resistor, as required by claim 55.

Koazechi fails to compensate for the shortcomings of Sawtell. Koazechi teaches the voltage difference DVBE between base-emitter voltages VBE20 and VBE24, which appears across resistor 2. Col. 4, lines 14-21. Resistor 2 of Koazechi is coupled to the emitter of transistor 24. Figure 2. Nowhere does Koazechi teach or suggest that a means for developing a current proportional to absolute temperature includes a resistor coupled to a base of a first bipolar transistor, a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities being formed across the resistor, as required by claim 55. Since neither Sawtell nor Koazechi teaches or suggests the limitations of claim 55, Applicants respectfully request that the rejection of claims 55-58 and all claims dependent thereon, be reversed.

Ground III:

Claims 1, 3, 7-26, 28-37, 55-57, and 59-60 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Akioka in combination with Koazechi.

In rejecting the claims, the Examiner engages in an examination that fails to establish a *prima facie* case of obviousness because the references fail to teach or suggest the claimed combination. See In re Nielson, 816 F.2d 1567, 1572, 2 USPQ2d (BNA) 1525, 1528 (Fed. Cir. 1987); see also In re Kahn, 441 F.3d 977, 986, 78 USPQ2d (BNA) 1329, 1335 (Fed. Cir. 2006).

In general, obviousness is a legal determination based on underlying factual inquiries. See Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1572-73, 24 USPQ2d (BNA) 1321, 1332-33 (Fed. Cir. 1992). Graham v. John Deere Co., 383 U.S. 1, 17 (1966) defines the factual inquiries utilized to evaluate the prior art. Specifically, the prior art is evaluated in terms of: (1) its scope and content; (2) the differences between the prior art and the claimed invention; (3) the level of ordinary skill in the art at the time the application was filed; and (4) objective, or secondary, evidence of nonobviousness such as commercial success, failure of others, long-felt need and unexpected results, which must be considered in reaching a conclusion of obviousness. See Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ (BNA) 459, 460 (1966); Panduit Corp. v. Dennison Mfg. Co., 810 F.2d 1561, 1566-67, 1 USPQ2d (BNA) 1593, 1595-96 (Fed. Cir. 1987); Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1573, 24 USPQ2d (BNA) 1321, 1333 (Fed. Cir. 1992).

In the present appeal, the issue relates to specific differences between the prior art and appealed claims. All claim limitations must be considered in the obviousness analysis. See Panduit Corp., 810 F.2d at 1576, 1 USPQ2d at 1603–04. None of the references, standing alone or in combination, teach all of the recited limitations.

Claim 26, 28-37, and 60

Regarding claim 26, Applicants respectfully maintain that Akioka, alone or in combination with Koazechi or other references of record, fails to teach or suggest that a

> base current is proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of a first bipolar transistor, the voltage difference being formed across a first resistor coupled to a base of the first bipolar transistor,

as required by claim 26. Akioka teaches forming a difference voltage between base-to-emitter voltages VBE of respective bipolar transistors Q1 and Q2 across a resistive element R2. See col. 4, lines 40-42. Resistive element R2 of Akioka is coupled between the emitter of bipolar

transistor Q2 and ground. See Figs. 2, 3, and 8. In addition, Akioka teaches that bipolar transistor Q8 is configured to generate a voltage VBE which is added to K*VT to provide an output voltage VREF free of temperature dependence. See col. 5, lines 1-4. The Office seems to argue that resistive element R3 of Akioka corresponds to the resistor of claim 26. However, R3 of Akioka is not coupled to the base of the first bipolar transistor, as required by claim 26. Akioka teaches that the current proportional to the thermal voltage VT flows through M4 and that this current also flows through the resistive element R3. See col. 4, line 63-col. 5, line 1. Nowhere does Akioka teach or suggest a base current proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of the first bipolar transistor, the voltage difference being formed across a first resistor coupled to a base of the first bipolar transistor, as required by claim 26.

Koazechi fails to compensate for the shortcomings of Akioka. Koazechi teaches the voltage difference DVBE between base-emitter voltages VBE20 and VBE24, which appears across resistor 2. See col. 4, lines 14-21. Resistor 2 of Koazechi is coupled to the emitter of transistor 24. See Fig. 2. Nowhere does Koazechi teach or suggest a base current proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of the first bipolar transistor, the voltage difference being formed across a first resistor coupled to a base of the first bipolar transistor, as required by claim 26. Thus, there is no teaching or suggestion to change the configuration R2 or R3 of Akioka to a configuration required by claim 26. Since Akioka, alone or in combination with other references of record, fails to teach or suggest the limitations of claim 26, Applicants respectfully request that the rejection of claim 26 and all claims dependent thereon be reversed.

Claim 3

Regarding claim 3, Applicants respectfully maintain that the Office fails to establish a *prima facie* case of obviousness. The Office action fails to provide a reference of record that teaches or suggests that

> a reference voltage produced by the voltage reference generator is proportional to a parabolic function of temperature,

as required by claim 3. Akioka teaches "a circuit for generating a constant voltage, free of dependence on temperature changes." See Abstract. Koazechi teaches generating a stable reference voltage with respect to changes in temperature. See col. 1, lines 9-17. Nowhere do the references of record teach or suggest a voltage reference generator generating a reference voltage that is proportional to a parabolic function of temperature, as required by claim 3. Rather, the Office impermissibly introduces hindsight into the obviousness analysis. In particular, the Office action implies that it would have been obvious to one of skill in the art at the time of invention to generate a reference voltage proportional to a parabolic function of temperature because a parabolic function of temperature function and its suitability for a voltage reference generator is known in the art. However, the Office fails to provide a reference to support this position. "'To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.'" W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). Since the Office fails to provide a reference that teaches or suggests a reference voltage produced by the voltage reference generator that is proportional to a parabolic function of temperature, Applicants respectfully request that the rejection of claim 3 be reversed.

Claim 1, 2, 7-25

Regarding claim 1, Applicants respectfully maintain that Akioka, alone or in combination with Koazechi or other references of record, fails to teach or suggest that

> the base current is proportional to a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities, the voltage difference being formed across the resistor coupled to the base of the first bipolar transistor,

as required by claim 1. Akioka teaches forming a difference voltage between base-to-emitter voltages VBE of respective bipolar transistors Q1 and Q2 across a resistive element R2. See col.

4, lines 40-42. Resistive element R2 of Akioka is coupled between the emitter of bipolar transistor Q2 and ground. See Figs. 2, 3, and 8. In addition, Akioka teaches that bipolar transistor Q8 is configured to generate a voltage VBE which is added to K*VT to provide an output voltage VREF free of temperature dependence. See col. 5, lines 1-4. The Office seems to argue that resistive element R3 of Akioka corresponds to the resistor of claim 1. However, R3 of Akioka is not coupled to have the voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities formed across that resistor, as required by claim 1. Akioka teaches that the current proportional to the thermal voltage VT flows through M4 and that this current also flows through the resistive element R3. See col. 4, line 63-col. 5, line 1. Nowhere does Akioka teach or suggest a bipolar transistor configured to amplify a base current of the first bipolar transistor, the base current being proportional to an absolute temperature, and a resistor coupled to the base of the bipolar transistor, wherein the base current is proportional to a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities, the voltage difference being formed across the resistor coupled to the base of the first bipolar transistor, as required by claim 1.

Koazechi fails to compensate for the shortcomings of Akioka. Koazechi teaches the voltage difference DVBE between base-emitter voltages VBE20 and VBE24, which appears across resistor 2. See col. 4, lines 14-21. Resistor 2 of Koazechi is coupled to the emitter of transistor 24. See Fig. 2. Nowhere does Koazechi teach or suggest a bipolar transistor configured to amplify a base current of the first bipolar transistor, the base current being proportional to an absolute temperature, and a resistor coupled to the base of the bipolar transistor, wherein the base current is proportional to a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities, the voltage difference being formed across the resistor coupled to the base of the first bipolar transistor, as required by claim 1. Thus, there is no teaching or suggestion to change the configuration R2 or R3 of Akioka to a configuration required by claim 1. Since Akioka, alone or in combination with other references of record, fails to teach or suggest the limitations of claim 1, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon be reversed.

Claim 55-58

Regarding claim 55, Applicants respectfully maintain that Akioka, alone or in combination with Koazechi or other references of record, fails to teach or suggest

> means for developing the current proportional to absolute temperature that includes a resistor coupled to a base of the first bipolar transistor, a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities being formed across the resistor,

as required by claim 55. Akioka teaches forming a difference voltage between base-to-emitter voltages VBE of respective bipolar transistors Q1 and Q2 across a resistive element R2. See col. 4, lines 40-42. Resistive element R2 of Akioka is coupled between the emitter of bipolar transistor Q2 and ground. See Figs. 2, 3, and 8. In addition, Akioka teaches that bipolar transistor Q8 is configured to generate a voltage VBE which is added to K*VT to provide an output voltage VREF free of temperature dependence. See col. 5, lines 1-4. The Office seems to argue that resistive element R3 of Akioka corresponds to the resistor of claim 55. However, R3 of Akioka is not coupled to have the voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities formed across that resistor, as required by claim 55. Akioka teaches that the current proportional to the thermal voltage VT flows through M4 and that this current also flows through the resistive element R3. See col. 4, line 63-col. 5, line 1. Nowhere does Akioka teach or suggest a means for developing the current proportional to absolute temperature that includes a resistor coupled to a base of the first bipolar transistor, a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities being formed across the resistor, as required by claim 55.

Koazechi fails to compensate for the shortcomings of Akioka. Koazechi teaches the voltage difference DVBE between base-emitter voltages VBE20 and VBE24, which appears across resistor 2. See col. 4, lines 14-21. Resistor 2 of Koazechi is coupled to the emitter of transistor 24. See Fig. 2. Nowhere does Koazechi teach or suggest a means for developing the

current proportional to absolute temperature that includes a resistor coupled to a base of the first bipolar transistor, a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities being formed across the resistor, as required by claim 55. Thus, there is no teaching or suggestion to change the configuration R2 or R3 of Akioka to a configuration required by claim 55. Since Akioka, alone or in combination with other references of record, fails to teach or suggest the limitations of claim 55, Applicants respectfully request that the rejection of claim 55 and all claims dependent thereon be reversed.

Claim 59

Regarding claim 59, Applicants respectfully maintain that Akioka, alone or in combination with Koazechi or other references of record, fails to teach or suggest that

> a base-collector voltage of a first bipolar transistor equals a voltage difference between two base-emitter voltages biased at different current densities,

as required by claim 59. Akioka teaches forming a difference voltage between base-to-emitter voltages VBE of respective bipolar transistors Q1 and Q2 across a resistive element R2. See col. 4, lines 40-42. Resistive element R2 is coupled between the emitter of bipolar transistor Q2 and ground. See Figs. 2, 3, and 8. In addition, Akioka teaches that bipolar transistor Q8 is configured to generate a voltage VBE which is added to K*VT to provide an output voltage VREF free of temperature dependence. See col. 5, lines 1-4. Akioka teaches that the current proportional to the thermal voltage VT flows through M4 and that this current also flows through the resistive element R3. See col. 4, line 63-col. 5, line 1. Nowhere does Akioka teach or suggest that a base-collector voltage of a first bipolar transistor equals a voltage difference between two base-emitter voltages biased at different current densities, as required by claim 59.

Koazechi fails to compensate for the shortcomings of Akioka. Koazechi teaches the voltage difference DVBE between base-emitter voltages VBE20 and VBE24, which appears across resistor 2. See col. 4, lines 14-21. Resistor 2 of Koazechi is coupled to the emitter of transistor 24. See Fig. 2. Nowhere does Koazechi teach or suggest that a base-collector voltage of a first bipolar transistor equals a voltage difference between two base-emitter voltages biased

at different current densities, as required by claim 59. Since Akioka, alone or in combination with other references of record, fails to teach or suggest the limitations of claim 59, Applicants respectfully request that the rejection of claim 59 and all claims dependent thereon be reversed.

Claim 29

Regarding claim 29, Applicants respectfully maintain that the Office fails to establish a *prima facie* case of obviousness. The Office action fails to provide a reference of record that teaches or suggests

> adjusting an effective slope of the reference voltage as a function of temperature according to the first resistor,

as required by claim 29. Akioka teaches "a circuit for generating a constant voltage, free of dependence on temperature changes." Abstract. Koazechi teaches generating a stable reference voltage with respect to changes in temperature. Col. 1, lines 9-17. Nowhere do the references of record teach or suggest adjusting an effective slope of the reference voltage as a function of temperature according to the first resistor, as required by claim 29. Rather, the Office impermissibly introduces hindsight into the obviousness analysis. "'To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.'" W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). Since the Office fails to provide a reference that teaches or suggests adjusting an effective slope of the reference voltage as a function of temperature according to a first resistor, Applicants respectfully request that the rejection of claim 29 be reversed.

CONCLUSION

For the at least the foregoing reasons, Applicants' presently claimed invention is not anticipated by the cited prior art and would not have been obvious to one of ordinary skill in the art under 35 U.S.C. § 103(a) in view of the cited prior art. Accordingly, this honorable Board is

respectfully requested to reverse the rejections of claims 1, 7-26, 28-37, 55-60 and to direct the claims of the present application to be issued.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

- ☐ deposited with the US Postal Service with sufficient postage as first class mail in an envelope addressed as shown above.
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Nicole Teitler Cave — Date: 3/5/07

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Respectfully submitted,

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CLAIMS APPENDIX

1. A voltage reference generator comprising:

a first bipolar transistor configured to amplify a base current of the first bipolar transistor, the base current being proportional to an absolute temperature, and

a resistor coupled to the base of the first bipolar transistor,

wherein the base current is proportional to a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities, the voltage difference being formed across the resistor.

3. The voltage reference generator, as recited in claim 1, wherein a reference voltage produced by the voltage reference generator is proportional to a parabolic function of temperature.

7. The voltage reference generator, as recited in claim 1, wherein a power supply coupled to the voltage reference generator is less than 1.7V.

8. The voltage reference generator, as recited in claim 7, wherein a power supply rejection ratio of the voltage reference generator is at least 60dB.

9. The voltage reference generator, as recited in claim 1, wherein a reference voltage generated is less than the bandgap voltage of silicon.

10. The voltage reference generator, as recited in claim 1, comprising:

a second bipolar transistor, providing one of the two base-emitter voltages; and

a voltage reference node receiving a voltage based at least in part on the voltage difference.

11. The voltage reference generator, as recited in claim 10, wherein a first current is based at least in part on the amplified base current of the first bipolar transistor.

12. The voltage reference generator, as recited in claim 10, wherein the first bipolar transistor provides the other of the two base-emitter voltages, and the second bipolar transistor operates at a current density different from the current density of the first bipolar transistor.

13. The voltage reference generator, as recited in claim 10, wherein the first bipolar transistor is a low-beta transistor.

14. The voltage reference generator, as recited in claim 13, wherein beta is less than ten.

15. The voltage reference generator, as recited in claim 13, wherein beta is less than five.

16. The voltage reference generator, as recited in claim 10, further comprising:
a circuit coupled to the voltage reference node, the circuit generating a first voltage, the first voltage proportional to a complement of the absolute temperature.

17. The voltage reference generator, as recited in claim 10, further comprising:
an operational amplifier maintaining effective equivalence of a voltage on a node coupled to the first bipolar transistor and a node coupled to the second bipolar transistor.

18. The voltage reference generator, as recited in claim 17, wherein a noise component on the voltage reference node is substantially equivalent to noise of the operational amplifier.

19. The voltage reference generator, as recited in claim 10, wherein the integrated circuit includes a maximum of one feedback path.

20. The voltage reference generator, as recited in claim 11, further comprising:
a current mirror coupled to the voltage reference node, the current mirror mirroring the first current without substantially amplifying the first current.

21. The voltage reference generator, as recited in claim 10, wherein the voltage is proportional to a parabolic function of temperature.

22. The voltage reference generator, as recited in claim 21, wherein the resistor has a value adjusting an effective slope of the reference voltage as a function of temperature.

23. The voltage reference generator, as recited in claim 10, wherein a power supply coupled to the voltage reference node is less than 1.7V.

24. The voltage reference generator, as recited in claim 23, wherein the power supply rejection ratio is at least 60dB.

25. The voltage reference generator, as recited in claim 10, wherein the voltage is less than the bandgap voltage of silicon.

26. A method for generating a reference voltage comprising:

developing a base current of a first bipolar transistor, the base current being proportional to absolute temperature;

amplifying the base current; and

generating a reference voltage based at least in part on the amplified base current,

wherein the base current is proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of the first bipolar transistor, the voltage difference being formed across a first resistor coupled to a base of the first bipolar transistor.

28. The method, as recited in claim 26, wherein the reference voltage is proportional to a parabolic function of temperature.

29. The method, as recited in claim 28, further comprising:

adjusting an effective slope of the reference voltage as a function of temperature according to the first resistor.

30. The method, as recited in claim 26, further comprising:

maintaining substantial equivalence of a voltage on a first node and a voltage on a second node with an operational amplifier, the first and second nodes being used to develop the base current.

31. The method, as recited in claim 26, further comprising:
mirroring the amplified current, the mirroring having an effective gain of one.

32. The method, as recited in claim 27, wherein the first bipolar transistor is a low-beta transistor.

33. The method, as recited in claim 32, wherein beta is less than ten.

34. The method, as recited in claim 32, wherein beta is less than five.

35. The method, as recited in claim 26, wherein the reference voltage is less than the bandgap voltage of silicon.

36. The method, as recited in claim 26, wherein a power supply coupled to the voltage reference node is less than 1.7V.

37. The method, as recited in claim 36, wherein the power supply rejection ratio is at least 60dB.

55. An apparatus comprising:
means for developing a current proportional to absolute temperature;
means for amplifying the current; and
means for generating a reference voltage based at least in part on the amplified current,
wherein the means for amplifying includes a first bipolar transistor, and
wherein the means for developing the current proportional to absolute temperature includes a resistor coupled to a base of the first bipolar transistor, a voltage difference between two base-emitter voltages of bipolar transistors configured to have different current densities being formed across the resistor.

56. The apparatus, as recited in claim 55, wherein the reference voltage varies according to a parabolic function of temperature.

57. The apparatus, as recited in claim 55, further comprising:

means for adjusting an effective slope of the reference voltage as a function of temperature.

58. The apparatus, as recited in claim 55, wherein the means for developing the current proportional to absolute temperature includes the means for amplifying current and the means for amplifying provides one of the two base-emitter voltages of bipolar transistors.

59. A voltage reference generator comprising:

a first bipolar transistor configured to amplify a base current of the first bipolar transistor, the base current being proportional to an absolute temperature,

wherein a base-collector voltage of the first bipolar transistor equals a voltage difference between two base-emitter voltages biased at different current densities.

60. The method, as recited in claim 26, wherein the first and second bipolar transistors are configured to have different current densities.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. § 1.130, 1.131, or 1.132 or any other evidence entered by the examiner and relied upon by appellant in the appeal.

RELATED APPEALS APPENDIX

There are no decisions rendered by a court or the Board in any proceeding identified above in the Related Appeals and Interferences section.